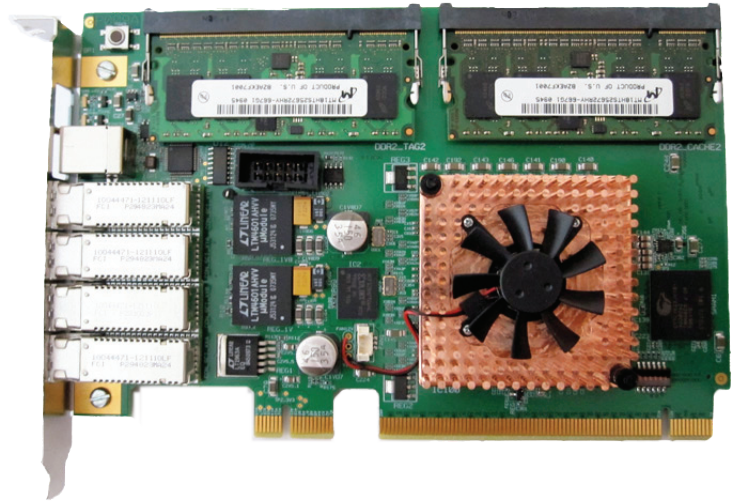


## Software Development Kit



## NumaConnect™ SDK

The NumaConnect SDK has been developed as a vehicle for customers to get early access to Numascale's groundbreaking cc-Numa technology. The SDK consists of a module that plugs into the HTX connector that can be found on AMD-based servers from some vendors.

The SDK adapter includes all the functional features of the NumaConnect technology. The SDK is based on an FPGA that holds the same logic design image as the NumaChip™ ASIC that is being developed for the high volume manufactured adapters while scalability and performance are limited by the FPGA.

The SDK is available for a limited set of customers that will be enrolled in Numascale's early adapter program. The SDK will be produced in limited volume and qualified customers will receive the SDK's on a first come, first serve basis.

The SDK can be configured in 1- or 2-D topologies (the ASIC also supports 3-D). The performance of the SDK is defined by the FPGA speed. The HT connection will run at 200MHz and the SERDES fabric lanes will run at 2.5GHz. System size with the SDK is flexible due to the scalable 2-D Torus topology. A 10 x 10 configuration (100 nodes) with 4-socket "Istanbul" 6-core processors will contain 2 400 processor cores. The Remote Cache RDIMM modules, the Fast Tag SRAM and cables and connectors are identical with the NumaChip ASIC-based volume production units.

Customers that purchase NumaConnect SDKs will receive new adapters with the NumaChip ASIC to replace the SDK as soon as this is available at no extra cost.

Performance measurements for the SDK will be irrelevant with respect to the performance of the volume production units with the NumaChip ASIC and will not be subject to publishing.

- Shared Memory
- Shared I/O
- Scalable, Directory Based Cache Coherence Protocol
- Write-back cache for Remote Data: 2 or 4 GigaBytes configurable
- ECC protected with background scrubbing of soft errors
- 16 coherent + 16 non-coherent outstanding memory transactions
- Support for single-image or multi-image OS partitions
- 2-way on-chip distributed switching for 1D or 2D Torus topologies
- HTX connected