NUMASCALE

Job Category: Engineering
Job Location: Ahmedabad, Gujarat, INDIA
Job Type: Experienced or New College Graduate Hire

1. ASIC Physical Design Engineer (Experience 2-5 years)

Job Description
Creates bottoms-up elements of chip design including but not limited to cell, and block level Semi-custom layouts, FUB-level floor plans, abstract view generation, RC extraction and schematic-to-layout verification, reliability verification and debug using phases of physical design development including parasitic extraction, custom polygon editing, auto place and route algorithms, floor planning, full-chip assembly, full-chip timing and verification. Troubleshoots a wide variety up to and including difficult design issues and applied proactive intervention. Knowledge of industry standard Auto Place and Route CAD tool, STA tool, Physical design methodologies.

Required Qualifications:
- BTech/BE/MTech/ME/MS - Electronics/Telecommunication/computer science or equivalent
- 2-5 years of Hands on experience doing Physical Design of complex blocks and/or FullChip designs.
- Should have worked on the entire PhyD Flow from netlist to GDS
- Expertise in Synopsys suite (IC Compiler, Primetime, Design Compiler)
- Expert in Synthesis to Tape-out flow & ECOs
- Layout design, Floor planning, P & R
- design rule checks (DRC), and Logical vs. Schematic (LVS) checks, RC extraction
- Fullchip timing, STA timing closure, Clock Tree Synthesis
- Expertise in scripting languages such as PERL, TCL.
- Ability to independently handle complex blocks to closure right from Synthesis
- Ability to communicate with architecture, RTL design and other remote teams
- Excellent verbal and written communication skills

2. ASIC Physical Design Engineer (Experience 0-2 years)

Job Description
Perform physical design of a ASIC blocks including floor planning, layout, place and route, clock tree and timing closure. You will be working closely with the physical design experts to ramp on the existing flow. You will be responsible to run complete physical design flow of a given block. You should be very strong in identifying the problems and propose/implement the solutions in given time frame to execute the planned delivery.

Required Qualifications:
- BTech/BE/MTech/ME/MS - Electronics/Telecommunication/computer science or equivalent
- 0-2 years of Hands on experience doing Physical Design of sub-blocks.
- Familiar with Synopsys suite (IC Compiler, Primetime, Design Compiler)
- Familiar with Synthesis to Tape-out flow

- Layout design, Floor planning, P & R
- design rule checks (DRC), and Logical vs. Schematic (LVS) checks, RC extraction
- Work effectively with a global team and be self-motivated
- Excellent verbal and written communication skills
- Expertise in scripting languages such as PERL, TCL.

About Numascale and Physical Design Team:

Numascale (www.numascale.com) is the central enabler of large scale data intensive computing solution in the industry. Developing ASIC component using Intel cache coherent technology that enables to build single node systems with high CPU socket count with large coherent memory foot print that produces highly efficient computing throughput. Numascale delivered the enabling technology for the world's largest computer running under one instance of the operating system, with more than 5000 cores and 21 Terabytes of RAM.

Scale-Up computing demand is growing in enterprise and in cloud segments. Numascale engineering team needs to grow to keep up with this computing paradigm shift. Numascale is looking for enthusiastic and passionate engineers who want to embrace the challenge and be part of the upcoming exciting world of Scale-Up computing. Join the team of highly energetic engineers who does not take "no" for an answer and always find the "yes" for any engineering solution to achieve the goals. You will be part of an open and flexible team with high degree of professional work ethic.

Please send your CV and application to: vb@numascale.com